Exhibit R-2, RDT&E Budget Item Justification: PB 2020 Office of the Secretary Of Defense	Date: February 2019
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 4: *Advanced Component Development & Prototypes (ACD&P)*	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*

COST ($ in Millions)	Prior Years	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
Total Program Element	0.000	147.481	522.950	542.421	-	542.421	232.447	244.070	245.624	250.706	Continuing	Continuing
291: *Joint Federated Assurance Center*	-	0.000	12.000	5.887	-	5.887	6.867	6.844	6.820	6.796	Continuing	Continuing
645: *Verification & Validation (V&V) Capabilities and Standards for Trust*	0.000	147.481	41.773	39.117	-	39.117	33.686	34.428	34.828	35.854	Continuing	Continuing
646: *New Trust Approach Development*	0.000	0.000	40.428	38.247	-	38.247	32.870	33.594	34.369	35.056	Continuing	Continuing
647: *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*	-	0.000	428.749	459.170	-	459.170	159.024	169.204	169.607	173.000	Continuing	Continuing

A. Mission Description and Budget Item Justification

This Program Element (PE) implements, maintains, and updates the DoD's long-term microelectronics strategy and places emphasis on incentivizing and proving new microelectronics technology solutions. In FY 2019 funding for the Joint Federated Assurance Center (JFAC) hardware and software assurance and integrity analysis activities and Microelectronic Innovation for National Security and Economic Competitiveness (MINSEC) activities were reallocated under Project 291 and Project 647, respectively.

This PE supports the 2018 National Defense Strategy's (NDS) line of effort to build a more lethal force through modernization of key capabilities and the NDS defense objective of establishing an unmatched twenty-first century National Security Innovation Base that effectively supports Department operations and sustains security and solvency.

Recognizing that a trusted and assured supply of microelectronics is a U.S. Government (USG)-wide concern, this activity will interface with interagency partners to take into account interagency requirements, opportunities for collaboration, and strategic decisions that can be made to limit the overall cost of these requirements to the USG. Its goal is to mitigate the Department of Defense (DoD)'s reliance on sole source foundries for trusted state-of-the-art (SOTA) microelectronics. It supports activities to ensure critical and sensitive integrated circuits are available to meet the DoD's needs. It refines strategies and management planning activities implementing three integrated, complementary solutions that: (1) protect the Intellectual Property (IP) of microelectronics components; (2) improve capabilities to evaluate and validate the trust and assurance of microelectronic parts and advance standards to incentivise the commercial marketplace to recognize hardware assurance as a competitive design standard; (3) develop and demonstrate alternative approaches to the DoD Trusted Foundry program to assure the microelectronics supply chain; and (4) provide

access to and leadership in advanced microelectronics that are vital to the national security and economic competitiveness for the USG in order to enable DoD and broader USG access to commercial SOTA microelectronics technology.

This activity is being led by the Under Secretary of Defense for Research and Engineering. This activity is conducted, in coordination with the JFAC Steering Committee and the Science and Technology (S&T) Advisory Board, by performers, such as the JFAC service providers, Defense Microelectronics Activity (DMEA), the Defense Advanced Research Programs Agency (DARPA), and other DoD and Intelligence Community S&T organizations and laboratories in the area of hardware assurance (HwA) and software assurance (SwA). It is integrating with, and supporting, the functions of the DoD Trusted Foundry Program, the Trusted Supplier accreditation program, JFAC, and related HwA and SwA S&T actions. This activity is also expected to maintain and update the DoD long-term microelectronics strategy based on feedback from the execution of this PE and enable and leverage commercial and academic relationships as necessary to fulfill this mission.

B. Program Change Summary ($ in Millions)	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total
Previous President's Budget	83.626	233.142	237.209	-	237.209
Current President's Budget	147.481	522.950	542.421	-	542.421
Total Adjustments	63.855	289.808	305.212	-	305.212
• Congressional General Reductions	-	-			
• Congressional Directed Reductions	-	-			
• Congressional Rescissions	-	-			
• Congressional Adds	66.000	291.000			
• Congressional Directed Transfers	-	-			
• Reprogrammings	-	-			
• SBIR/STTR Transfer	-1.984	-			
• FFRDC Reduction	-0.161	-1.192	-	-	-
• Other Program Adjustments	-	-	-0.675	-	-0.675
• Adjustment for MINSEC Project 647	-	-	302.000	-	302.000
• Adjustment for JFAC Project 291	-	-	3.887	-	3.887

Congressional Add Details ($ in Millions, and Includes General Reductions)	FY 2018	FY 2019
Project: 291: *Joint Federated Assurance Center*		
Congressional Add: *Joint Federated Assurance Center*	-	10.000
Congressional Add Subtotals for Project: 291	-	10.000
Project: 645: *Verification & Validation (V&V) Capabilities and Standards for Trust*		
Congressional Add: *New Trust Approach Development*	66.000	-
Congressional Add Subtotals for Project: 645	66.000	-

Exhibit R-2, RDT&E Budget Item Justification: PB 2020 Office of the Secretary Of Defense	Date: February 2019
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide I* BA 4: *Advanced Component Development & Prototypes (ACD&P)*	**R-1 Program Element (Number/Name)** PE 0604294D8Z *I Trusted and Assured Microelectronics*

Congressional Add Details ($ in Millions, and Includes General Reductions)	FY 2018	FY 2019
Project: 646: *New Trust Approach Development*		
Congressional Add: *New Trust Approach Development*	0.000	-
Congressional Add Subtotals for Project: 646	0.000	-
Project: 647: *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*		
Congressional Add: *Next Generation Microelectronics*	0.000	281.000
Congressional Add Subtotals for Project: 647	0.000	281.000
Congressional Add Totals for all Projects	66.000	291.000

Change Summary Explanation

FY 2019 funding in the amount of $291.000 million was added to support acceleration efforts for MINSEC, JFAC, and strategic radiation-hardening activities. In FY 2020, $302.000 million was added to provide access and assurance to domestic microelectronics production capabilities under Project 647, and $3.887 million was added to increase JFAC-related efforts under Project 291.

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*	Project (Number/Name) 291 / *Joint Federated Assurance Center*	

COST ($ in Millions)	Prior Years	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
291: *Joint Federated Assurance Center*	-	0.000	12.000	5.887	-	5.887	6.867	6.844	6.820	6.796	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project funds the operation and software assurance support to DoD programs and organizations of the Joint Federated Assurance Center (JFAC), established in National Defense Authorization Act (NDAA) Sec 937, to increase the DoD's software assurance (SwA) by providing engineering tools, technical services, best-practices, innovative technologies and other assistance to programs to detect, assess, prioritize, and mitigate vulnerabilities from malicious software attacks and assurance against supply chain exploitation vulnerabilities. The JFAC will provide capabilities for programs to keep assessment findings throughout the life cycle of their systems for data mining (e.g., documentation on rationale for previous mitigation decisions). The collaboration between the JFAC and program offices will help mitigate existing and emerging critical threats and vulnerabilities in software available to all DoD programs. JFAC efforts will continue to maintain infrastructure services and staff for the Joint Federated Assurance Center-Coordination Center (JFAC-CC) for enabling the centralized assurance repository, software assurance contract language, software assurance metrics, the JFAC Ticketing System, software assurance tool license distribution, help-desk, and hard problem analysis. It will also provide for implementation of the science and technology portal at the JFAC website to make directly available to programs and organizations advanced technology solutions from Defense Advanced Research Projects Agency (DARPA), Intelligence Advanced Research Projects Agency (IARPA), Defense Innovation Unit (DIU), and Software Engineering Institute (SEI) and other S&T providers.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
Title: Joint Federated Assurance Center (JFAC)	0.000	2.000	5.887
Description: This project's activities will enhance the use of software, hardware, and firmware assurance tools, techniques, and procedures directly with programs and organizations, throughout the life cycle. JFAC provides a common forum in DoD for assurance best practices, community dialog on assurance, access to new technology via the S&T portal, and a ticketing system to connect programs with assurance service providers, ask for hard problem analysis, or just ask for help. In addition, the Assessment Knowledge Base (AKB) will continue to be updated from program comments to retain all program and organization assessment data and a suite of data mining and reporting tools usable by a program throughout the life cycle.			
FY 2019 Plans: • Mature JFAC tools, technology and talent capabilities and capacity. • Maintain infrastructure services and staff for the JFAC-CC, enabling the centralized assurance repository, assurance contract language, metrics, SwA tool license distribution, help-desk, and hard problem analysis and provide to all DoD programs and organizations at no cost. • Incorporate S&T, DARPA, IARPA, DIU, and SEI products into the JFAC website for direct access by programs.			

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 291 / *Joint Federated Assurance Center*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
• Develop best practices, and relationships with industry. ***FY 2020 Plans:*** • Maintain infrastructure services and staff for the JFAC-CC, enabling the centralized assurance repository, assurance contract language, metrics, SwA tool license distribution, help-desk, and hard problem analysis and provide to all DoD programs and organizations at no cost. • Incorporate S&T, DARPA, IARPA, DIU, and SEI products into the JFAC website for direct access by programs. • Develop best practices, and relationships with industry. ***FY 2019 to FY 2020 Increase/Decrease Statement:*** Funding of $2.000 million transferred from PE 0603826D8Z P826 to PE 0604294D8Z P291 beginning in FY 2019. Increase in FY 2020 supports additional software assurance efforts.			
Accomplishments/Planned Programs Subtotals	0.000	2.000	5.887

	FY 2018	FY 2019
Congressional Add: Joint Federated Assurance Center	-	10.000
FY 2019 Plans: • Expand JFAC capabilities to more effectively identify and mitigate software and hardware cyber security vulnerabilities in DoD weapons systems and networks. • Enable JFAC to develop offense-defense interaction analytical capabilities to investigate a variety of threat capabilities and assess resulting system and network vulnerabilities. • In a joint service context, enable JFAC to conduct advanced scientific research to identify and mitigate cyber threats to software and hardware in DoD weapons systems and networks.		
Congressional Adds Subtotals	-	10.000

C. Other Program Funding Summary ($ in Millions)

Line Item	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
• O&M (CIVPAY): *0303140D8Z*	0.000	0.000	1.113	0.000	1.113	1.133	1.156	1.180	1.204	Continuing	Continuing

Remarks

D. Acquisition Strategy

N/A

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 291 / *Joint Federated Assurance Center*

E. Performance Metrics

Performance for this project is monitored in the following ways:

- Increases in throughput in current JFAC service providers, and coordination of the stand-up of additional assurance capability and capacity as Service funding allows.
- Increased Probability of Detection of mission software vulnerabilities.
- Decreased cost to evaluate components.
- Decreased time to evaluate components.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*	Project (Number/Name) 291 / *Joint Federated Assurance Center*	

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2018 Cost	FY 2018 Award Date	FY 2019 Cost	FY 2019 Award Date	FY 2020 Base Cost	FY 2020 Base Award Date	FY 2020 OCO Cost	FY 2020 OCO Award Date	FY 2020 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
Joint Federated Assurance Center	MIPR	Army, Navy, Air Force : Various	-	-		12.000	Jan 2019	5.887	Jan 2020	-		5.887	Continuing	Continuing	2.000
		Subtotal	-	-		12.000		5.887		-		5.887	Continuing	Continuing	N/A

	Prior Years	FY 2018		FY 2019		FY 2020 Base		FY 2020 OCO		FY 2020 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	-		12.000		5.887		-		5.887	Continuing	Continuing	N/A

Remarks

Exhibit R-4, RDT&E Schedule Profile: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 291 / *Joint Federated Assurance Center*

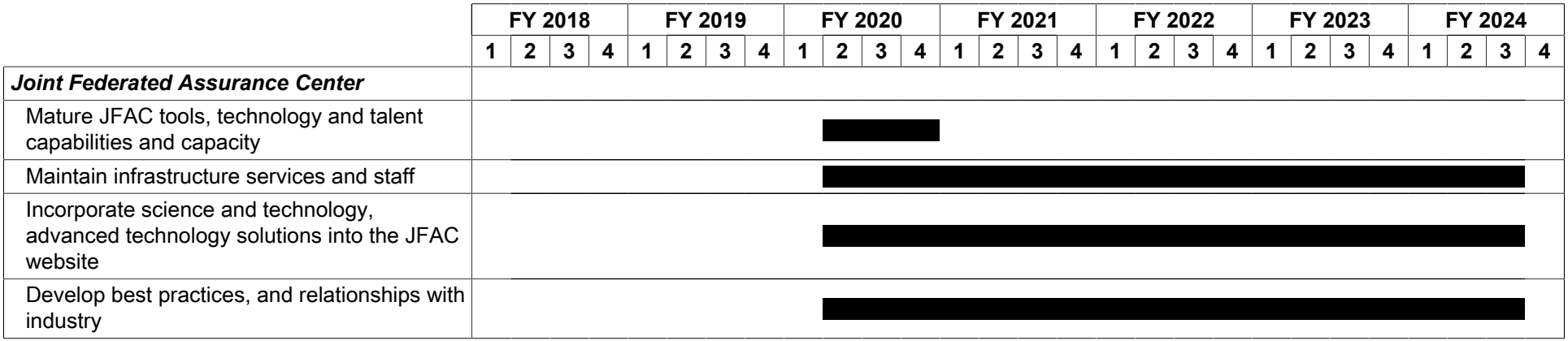

Exhibit R-4A, RDT&E Schedule Details: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 291 / *Joint Federated Assurance Center*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
Joint Federated Assurance Center				
Mature JFAC tools, technology and talent capabilities and capacity	2	2020	4	2020
Maintain infrastructure services and staff	2	2020	3	2024
Incorporate science and technology, advanced technology solutions into the JFAC website	2	2020	3	2024
Develop best practices, and relationships with industry	2	2020	3	2024

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*	Project (Number/Name) 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*	

COST ($ in Millions)	Prior Years	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
645: *Verification & Validation (V&V) Capabilities and Standards for Trust*	0.000	147.481	41.773	39.117	-	39.117	33.686	34.428	34.828	35.854	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project improves microelectronics test and verification methodologies in support of verifying the trust and assurance of parts and develops standards and practices to foster commercial development of secure, trusted and assured parts. Verification and test technologies are required to provide direct program support for microelectronics assurance verification when DoD Trusted Foundry Program options are not available. Core technical laboratories and other HwA and SwA capabilities are chartered as a JFAC to provide this support. Out-year demands will require an increase in capacity, which will take the form of additional personnel and/or equipment to permit scaling of microelectronics assessment capabilities. Challenges have been identified, to include the ability to analyze leading-edge technology nodes (<45 nanometers (nm)), throughput/time required for analysis, ability to analyze third-party IP contained in microelectronic components, and analysis of non-application specific integrated circuit (ASIC) components that are increasingly being used for agility, e.g., Field-Programmable Gate Arrays (FPGAs). This project addresses these gaps in current technical capabilities, in coordination with the JFAC, which prioritizes this investment as required to meet the realized and projected out-year demand for JFAC services. Three capability areas core to microelectronics analysis and verification will be improved:

- Physical verification, i.e., destructive analysis of integrated circuits and printed circuit boards.
- Functional analysis, i.e., non-destructive screening/verification of select, critical parts.
- Design verification, i.e., verification/assurance of designs, IP, netlists, bitstreams, firmware, etc.

These improvements address two primary attributes: (1) technical capability including laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) the capacity to perform microelectronics assessments.

This project develops and matures assurance mitigations, evaluates the effectiveness of protections of IP in support of integrity, and develops and validates obfuscation and disaggregation technologies. The project will address physical validation tool and capability development, design software validation tool development, counterfeit detection and imaging techniques, and system vulnerability assessments and testbeds.

This project also develops standards and practices in support of assured designs and supply chains and formal relationships with industry to foster commercial development of secure, trusted, and assured parts and for acquisition of USG access to proprietary designs, software, development, and quality assurance processes and test procedures to develop practices that minimize security flaws in designs and facilitate verification. Two capability areas that are core to improved commercial designs will be improved, i.e., assured designs and supply chains.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
Title: Verification & Validation (V&V) Capabilities and Standards for Trust	40.449	41.773	39.117

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
Description: The JFAC will: (1) improve its microelectronics test and verification methodologies in support of verifying trust and assurance of parts and (2) develop standards/practices to foster commercial development of secure, trusted and assured parts. ***FY 2019 Plans:*** Verification and test technologies activities will include: • Improvements to the core JFAC's (1) technical capability, through the procurement of laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) capacity to perform microelectronics assessments. FY 2019 and out-year demands will require an increase in capacity supporting weapon system program engagement, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities. • Testing in support of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) initiatives. • Strategic radiation hardened electronics council (SRHEC) coordination. • Strategic radiation support of radio frequency and optoelectronic devices. • Enhancement of automation and standard processes needed to increase the throughput of information produced by individual JFAC laboratory tools as well as to facilitate information sharing across the families of tools used for analysis and testing. • Research into qualification concerns regarding strategic radiation hardened parts from state of the art (SOTA) and state of the practice (SOTP) foundries. • Development of common subject matter expert (SME) training and protocols based on the existing tool base, to include both commercial and USG-developed tools. • Funding for additional SME support in each core laboratory in support of the microelectronics trust verification and other JFAC-related work. • Increased direct program support focused on addressing technical gaps and assurance-related findings. Standards and practices activities will include: • Development of standards and best practices, and relationships with industry, to foster commercial development of secure, trusted and assured parts. • Establishment of formal relationships with FPGA vendors and other key commercial suppliers to improve device and IP security. • Acquisition of USG access to proprietary designs, software, development, and quality assurance processes and test procedures to develop design practices that minimize security flaws and facilitate verification. • Establishment of USG and industry working groups to develop test procedures to validate the assurance of designs. • Documentation and promulgation of security-enhancing design practices across the USG, industry, and academia. • Development of industry-wide standards and practices to establish a common understanding of what constitutes assured hardware, software, and firmware at both the component and system level.			

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
• Development of a common lexicon for secure hardware, software, and firmware in collaboration with the Committee for National Security Systems, National Institute of Standards and Technology, and the broader USG, industry, and academia. • Definition of supply chain controls for assured chain of custody for critical and other microelectronics devices and IP. • Development of security training and education of USG and industry system security engineers and material managers on supply chain and life-cycle management best practices using agreed-upon language, standards, and practices. • Alignment of DoD Instruction 5200.44 (Protection of Mission Critical Functions to Achieve Trusted Systems and Networks (TSN)), and other related policies and guidance, with other USG, e.g., National Institute of Standards and Technology (NIST) 800-161 (Supply Chain Risk Management Practices for Federal Information Systems and Organizations), and industry standards identifying and addressing gaps in definition and criteria and establishing accepted levels of supplier and part assurance.			
FY 2020 Plans: Continuation of FY 2019 verification and test technologies activities including: • Improvements to the core JFAC's (1) technical capability, through the procurement of laboratory equipment, IP, analysis tools, such as imaging software, and highly skilled tradecraft, and (2) capacity to perform microelectronics assessments. FY 2019 and out-year demands will require an increase in capacity supporting weapon system program engagement, which will take the form of additional personnel and/or equipment to permit scaling of assessment capabilities. • Testing in support of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) initiatives. • Strategic radiation hardened electronics council (SRHEC) coordination. • Strategic radiation support of radio frequency and optoelectronic devices. • Enhancement of automation and standard processes needed to increase the throughput of information produced by individual JFAC laboratory tools as well as to facilitate information sharing across the families of tools used for analysis and testing. • Research into qualification concerns regarding strategic radiation hardened parts from state of the art (SOTA) and state of the practice (SOTP) foundries. • Development of common subject matter expert (SME) training and protocols based on the existing tool base, to include both commercial and USG-developed tools. • Funding for additional SME support in each core laboratory in support of the microelectronics trust verification and other JFAC-related work. • Increased direct program support focused on addressing technical gaps and assurance-related findings. Continuation of FY 2019 standards and practices activities including: • Development of standards and best practices, and relationships with industry, to foster commercial development of secure, trusted and assured parts. • Establishment of formal relationships with FPGA vendors and other key commercial suppliers to improve device and IP security.			

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
• Acquisition of USG access to proprietary designs, hardware, software, development, and quality assurance processes and test procedures to develop design practices that minimize security flaws and facilitate verification. • Establishment of USG and industry working groups to develop test procedures to validate the assurance of designs. • Documentation and promulgation of security-enhancing design practices across the USG, industry, and academia. • Development of industry-wide standards and practices to establish a common understanding of what constitutes assured hardware, software, and firmware at both the component and system level. • Development of a common lexicon for secure hardware, software, and firmware in collaboration with the Committee for National Security Systems, National Institute of Standards and Technology, and the broader USG, industry, and academia. • Definition of supply chain controls for assured chain of custody for critical and other microelectronics devices and IP. • Development of security training and education of USG and industry system security engineers and material managers on supply chain and life-cycle management best practices using agreed-upon language, standards, and practices. • Alignment of DoD Instruction 5200.44 (Protection of Mission Critical Functions to Achieve Trusted Systems and Networks (TSN)), and other related policies and guidance, with other USG, e.g., NIST 800-161 (Supply Chain Risk Management Practices for Federal Information Systems and Organizations), and industry standards identifying and addressing gaps in definition and criteria and establishing accepted levels of supplier and part assurance. ***FY 2019 to FY 2020 Increase/Decrease Statement:*** Level of effort is consistent between FY 2019 and FY 2020. Small changes reflect minor budget fluctuations.			
Title: New Trust Approach Development ***Description:*** This project's activities will mature and evaluate assurance technologies and techniques through efforts that may include the conduct of studies and Broad Agency Announcements (BAAs) and other efforts to coordinate research programs across USG R&D organizations, academia, and industry. In addition, the JFAC will initiate the conduct of identified acquisition program pilots and technology demonstrations in coordination with research programs across government R&D organizations, academia and industry. Note: Execution of these funds in FY 2018 is under project code 646.	41.032	-	-
Accomplishments/Planned Programs Subtotals	81.481	41.773	39.117

	FY 2018	FY 2019
Congressional Add: New Trust Approach Development	66.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

	FY 2018	FY 2019
FY 2018 Accomplishments: • Initiated development of an advanced technology center for next-generation artificial intelligence systems including standing up an intellectual property library. • Initiated modernization enhancements for 90 nanometer (nm) to 65nm/45nm radiation-hardened semiconductor fabrication at a government foundry. • Purchased and began installation of an electron-beam lithography tool at a government laboratory. • Evaluated state-of-the-art integrated chip (processor) for use in real-world DoD and other agency applications. • Awarded contract for advanced prototype development project using complementary metal oxide semiconductor photo diode arrays in collaboration with two commercial foundries. Note: Execution of these funds in FY 2018 is under project code 646.		
Congressional Adds Subtotals	66.000	-

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

N/A

D. Acquisition Strategy

NA

E. Performance Metrics

Performance for this project is monitored in the following ways:

• Increases in throughput in current JFAC laboratories, and stand-up of additional capability and capacity as required, so that at least two laboratories will have capability in physical verification, functional analysis, and design verification to increase the DoD's overall microelectronics trust verification and test capacity for analysis of parts.
• Increased Probability of Detection of malicious insertion and/or counterfeit parts.
• Decreased cost to evaluate components.
• Decreased time to evaluate components.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*	

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2018 Cost	FY 2018 Award Date	FY 2019 Cost	FY 2019 Award Date	FY 2020 Base Cost	FY 2020 Base Award Date	FY 2020 OCO Cost	FY 2020 OCO Award Date	FY 2020 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
V&V Capabilities and Standards for Trust	MIPR	Various (Air Force, Army, Navy, NSA) : Various	-	147.481	Mar 2018	41.773	Mar 2019	39.117	Mar 2020	-		39.117	Continuing	Continuing	-
		Subtotal	-	147.481		41.773		39.117		-		39.117	Continuing	Continuing	N/A

Remarks

N/A

	Prior Years	FY 2018		FY 2019		FY 2020 Base		FY 2020 OCO		FY 2020 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	147.481		41.773		39.117		-		39.117	Continuing	Continuing	N/A

Remarks

NA

Exhibit R-4, RDT&E Schedule Profile: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

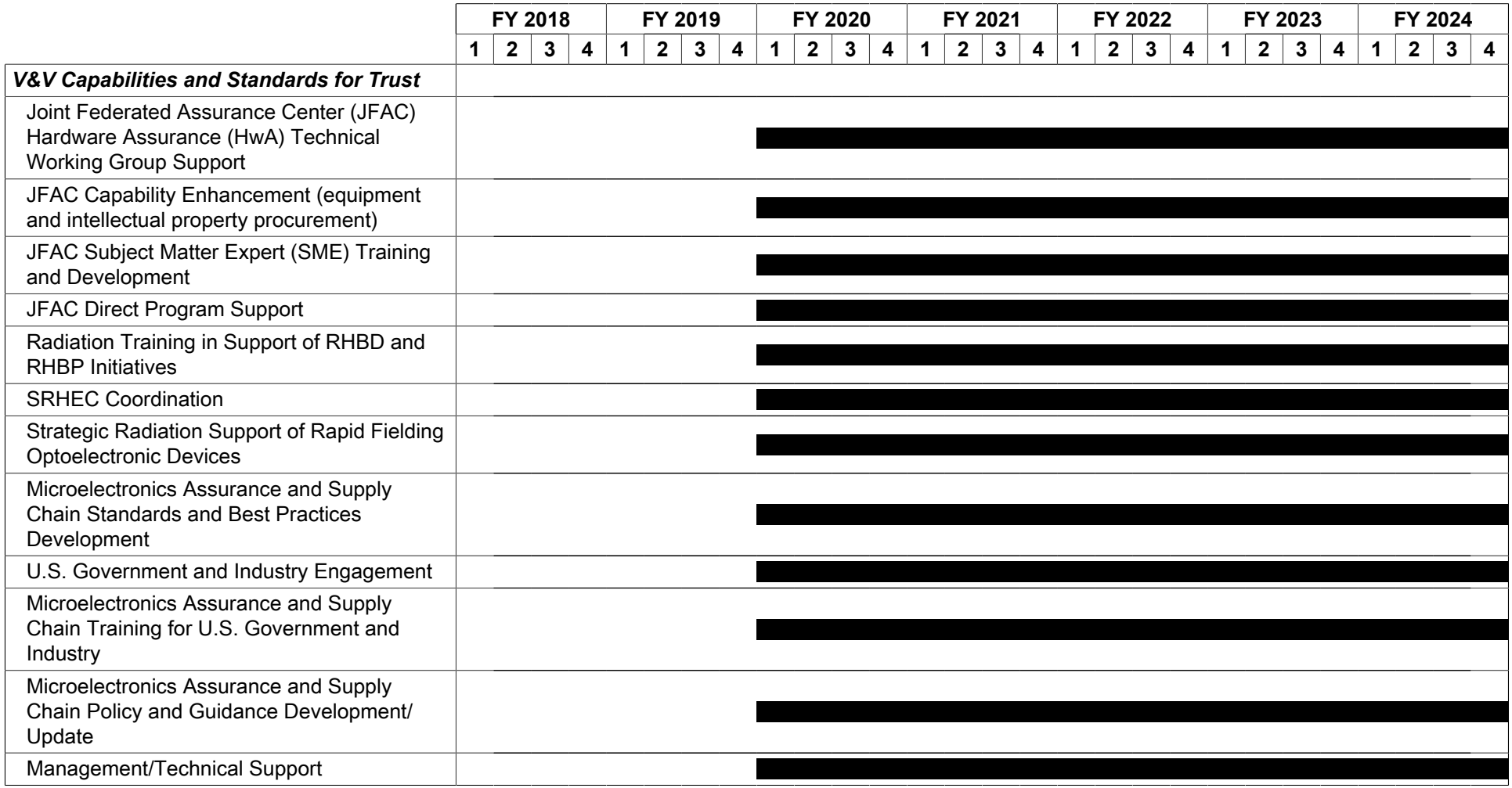

Exhibit R-4A, RDT&E Schedule Details: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 645 / *Verification & Validation (V&V) Capabilities and Standards for Trust*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
V&V Capabilities and Standards for Trust				
Joint Federated Assurance Center (JFAC) Hardware Assurance (HwA) Technical Working Group Support	1	2020	4	2024
JFAC Capability Enhancement (equipment and intellectual property procurement)	1	2020	4	2024
JFAC Subject Matter Expert (SME) Training and Development	1	2020	4	2024
JFAC Direct Program Support	1	2020	4	2024
Radiation Training in Support of RHBD and RHBP Initiatives	1	2020	4	2024
SRHEC Coordination	1	2020	4	2024
Strategic Radiation Support of Rapid Fielding Optoelectronic Devices	1	2020	4	2024
Microelectronics Assurance and Supply Chain Standards and Best Practices Development	1	2020	4	2024
U.S. Government and Industry Engagement	1	2020	4	2024
Microelectronics Assurance and Supply Chain Training for U.S. Government and Industry	1	2020	4	2024
Microelectronics Assurance and Supply Chain Policy and Guidance Development/ Update	1	2020	4	2024
Management/Technical Support	1	2020	4	2024

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	R-1 Program Element (Number/Name) PE 0604294D8Z / *Trusted and Assured Microelectronics*	Project (Number/Name) 646 / *New Trust Approach Development*	

COST ($ in Millions)	Prior Years	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
646: *New Trust Approach Development*	0.000	0.000	40.428	38.247	-	38.247	32.870	33.594	34.369	35.056	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project funds a program of research to develop the next generation, technology-driven approach to microelectronics trust and assurance, to include state-of-the-art (SOTA) microelectronics, to ensure continued access to SOTA microelectronic technologies while maintaining the required level of assurance in all environments. DoD's ability to access commercial technology for its custom, secure, trusted and assured needs is diminishing as SOTA suppliers become fewer and more focused on serving the global commercial market. DoD's technology needs are broad, and relying on a single source supplier is not feasible. Alternative, advanced manufacturing methods, technologies, and design tools are needed to produce secure, trusted and assured SOTA parts from commercial sources and to preserve access to these advanced nodes while protecting DoD and Defense Industrial Base intellectual property (IP) from exploitation. It is also intended to dramatically improve the capabilities of the JFAC with regard to verification and validation of SOTA microelectronics assurance.

This program of research will develop innovative design, manufacturing, imaging, tagging, and control and assessment approaches for protecting DoD's microelectronics supply chain and IP, including alternatives for trusted and assured strategic radiation-hardened electronics in advanced technology nodes for next-generation strategic systems, obfuscation and disaggregation technology development, and other assurance mitigations. It will develop advanced imaging technologies and forensics, Design for Assurance techniques, active hardware assurance controls, electronic component markers, and a data and analysis capability to enable auditing and independent verification and validation of commercial designs. It also develops, demonstrates, and implements concepts for the cost-effective production of custom microelectronics in low volumes and protection of sensitive IP from exploitation.

Assurance technologies that can be applied in a broad range of trusted and commercial environments can mitigate the risk associated with sole-source suppliers and increase the Government's ability to leverage commercial capabilities. The suite of developed technologies, e.g., alternative manufacturing methods and design tools, will enable DoD to obfuscate the purpose of sensitive devices, verify their origin and function, and protect sensitive IP from exploitation even while using the global supply chain for most hardware. In cases where the risk involved precludes that level of commercial collaboration, low-volume manufacturing technologies developed under this project would permit DoD to more cheaply produce low volumes of sensitive microelectronics in trusted environments. The project would also support using a repository of vetted third-party IP and electronic data automation (EDA) tools to expedite circuit design and transition promising technologies to use.

This project initially received additional funding in FY 2019 to support Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) efforts in the following focus areas: capture and secure microelectronics R&D; new microelectronics development, demonstration, and capability insertion; radiation hardening by process (RHBP) and radiation hardening by design (RHBD); and radio frequency (RF) and optoelectronics. In FY 2019, funding for those MINSEC activities was reallocated from Project Number 646 to Project Number 647.

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
Title: New Trust Approach Development	0.000	40.428	38.247

Description: This project's activities will mature and evaluate assurance technologies and techniques through efforts that may include the conduct of studies and Broad Agency Announcements (BAAs) and other efforts to coordinate research programs across USG R&D organizations, academia, and industry.

In addition, the JFAC will initiate the conduct of identified acquisition program pilots and technology demonstrations in coordination with research programs across government R&D organizations, academia and industry.

FY 2019 Plans:
This project will engage early on with potential stakeholders to identify potential transition issues and aid in transition through joint collaboration between research teams and stakeholders with a focus on evaluations of prototypes, test articles and beta versions of tools, IP, techniques, methods, etc. and their use in operationally-realistic scenarios.

Primary efforts will include the following:

- Reducing-to-practice technologies enabling assured (1) design, (2) access, (3) component integrity and (4) IP protection.
- Assured design demonstration and evaluation.
- Systems security analysis for assurance of microelectronics in DoD missions.
- Analog test chip fabrication.
- Advanced chip interconnection development to eliminate wire bonding and improve functional performance.
- Printed circuit board (PrCB) design confirmation tool development.
- Application-specific integrated circuit (ASIC) netlist analysis capability development.
- Field programmable gate array (FPGA) analyses tool development.
- Identification of non-invasive measurement techniques at the die/wafer level to provide increased hardware assurance.

Primary activities in FY 2019 will continue the development of these technologies, followed by transition of these capabilities to new programs in the fiscal years that follow under PE 0605294D8Z.

FY 2020 Plans:
Continuation of FY 2019 activities including the following:

- Reducing-to-practice technologies enabling assured (1) design, (2) access, (3) component integrity and (4) IP protection.
- Assured design demonstration and evaluation.
- Systems security analysis for assurance of microelectronics in DoD missions.

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
• Analog test chip fabrication. • Advanced chip interconnection development to eliminate wire bonding and improve functional performance. • Printed circuit board (PrCB) design confirmation tool development. • Application-specific integrated circuit (ASIC) netlist analysis capability development. • Field programmable gate array (FPGA) analyses tool development. • Identification of non-invasive measurement techniques at the die/wafer level to provide increased hardware assurance. ***FY 2019 to FY 2020 Increase/Decrease Statement:*** In FY 2019, funding for MINSEC activities was re-allocated from Project Number 646 to Project Number 647.			
Accomplishments/Planned Programs Subtotals	0.000	40.428	38.247

	FY 2018	FY 2019
Congressional Add: New Trust Approach Development	0.000	-
FY 2018 Accomplishments: • Initiated development of an advanced technology center for next-generation artificial intelligence systems including standing up an intellectual property library. • Initiated modernization enhancements for 90 nanometer (nm) to 65nm/45nm radiation-hardened semiconductor fabrication at a government foundry. • Purchased and began installation of an electron-beam lithography tool at a government laboratory. • Evaluated state-of-the-art integrated chip (processor) for use in real-world DoD and other agency applications. • Awarded contract for advanced prototype development project using complementary metal oxide semiconductor photo diode arrays in collaboration with two commercial foundries.		
Congressional Adds Subtotals	0.000	-

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

N/A

D. Acquisition Strategy

N/A

E. Performance Metrics

Performance for this project is monitored in the following ways:

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

• Enhanced capability in physical verification, functional analysis, and design verification.
• Increased Probability of Detection of malicious insertion and/or counterfeit parts.
• Effectiveness of developed technologies, as measured by:
- The speed and reliability of new validation and verification techniques in identifying known microelectronics issues (e.g., tampering) in laboratory and non-laboratory situations.
- Successful demonstration of advanced, alternative manufacturing techniques, such as disaggregated manufacturing.
- Resilience of microelectronics protected by new trust approach technologies in red teaming exercises.
• Adoption of next-generation commercial technologies, as measured by:
- The number of DoD and other USG programs employing assured access to SOTP and SOTA technologies, design approaches, and best practices developed in cooperation with commercial partners.
- The volume and criticality of components employing these technologies, design approaches, or best practices.
- Promulgation in DoD guidance and program protection plans.
• Commercial partnerships established for, or enhanced by, the development and manufacture of DoD microelectronics using next-generation assurance technologies.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2018 Cost	FY 2018 Award Date	FY 2019 Cost	FY 2019 Award Date	FY 2020 Base Cost	FY 2020 Base Award Date	FY 2020 OCO Cost	FY 2020 OCO Award Date	FY 2020 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
New Trust Approach Development	MIPR	Various (DARPA, Air Force, Army, Navy, NSA) : Various	-	0.000		40.428	Mar 2019	38.247	Mar 2020	-		38.247	Continuing	Continuing	-
		Subtotal	-	0.000		40.428		38.247		-		38.247	Continuing	Continuing	N/A

	Prior Years	FY 2018		FY 2019		FY 2020 Base		FY 2020 OCO		FY 2020 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	0.000		40.428		38.247		-		38.247	Continuing	Continuing	N/A

Remarks

NA

Exhibit R-4, RDT&E Schedule Profile: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

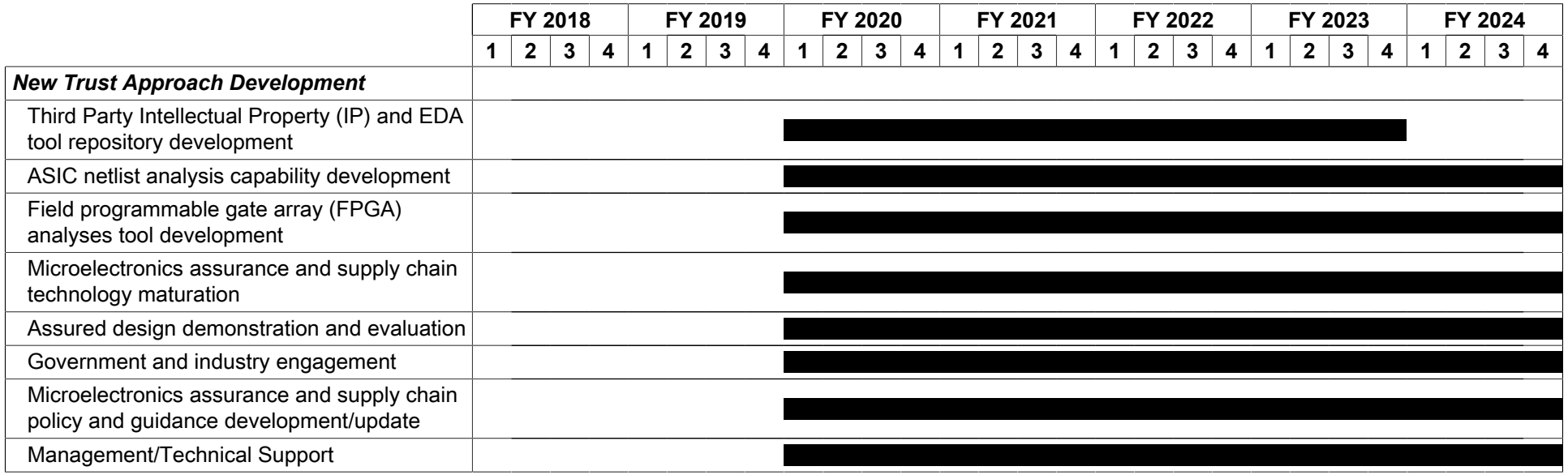

Exhibit R-4A, RDT&E Schedule Details: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 646 / *New Trust Approach Development*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
New Trust Approach Development				
Third Party Intellectual Property (IP) and EDA tool repository development	1	2020	4	2023
ASIC netlist analysis capability development	1	2020	4	2024
Field programmable gate array (FPGA) analyses tool development	1	2020	4	2024
Microelectronics assurance and supply chain technology maturation	1	2020	4	2024
Assured design demonstration and evaluation	1	2020	4	2024
Government and industry engagement	1	2020	4	2024
Microelectronics assurance and supply chain policy and guidance development/update	1	2020	4	2024
Management/Technical Support	1	2020	4	2024

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense			Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*	

COST ($ in Millions)	Prior Years	FY 2018	FY 2019	FY 2020 Base	FY 2020 OCO	FY 2020 Total	FY 2021	FY 2022	FY 2023	FY 2024	Cost To Complete	Total Cost
647: *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*	-	0.000	428.749	459.170	-	459.170	159.024	169.204	169.607	173.000	Continuing	Continuing
Quantity of RDT&E Articles	-	-	-	-	-	-	-	-	-	-		

A. Mission Description and Budget Item Justification

This project supports the DoD microelectronics strategy by ensuring the availability of and access to the advanced, assured microelectronics that are critical for DoD and national security systems. It will support the development and delivery of tools to protect the intellectual property (IP) confidentiality and integrity for a broad range of systems and missions and will provide a path for the production of these articles. It will allow the DoD to 1) maintain technological leadership and a secure domestic microelectronics ecosystem; 2) promote access to all necessary current and future semiconductor technologies, including design, fabrication, packaging, and testing, from a robust base of suppliers; 3) provide multiple options for programs and the defense industrial base to quickly upgrade microelectronic components; 4) create a competitive industrial base of microelectronics suppliers that can rapidly adjust to the dynamics of the industry including the initiation of modernization pilots with DoD programs and industry to deliver new capabilities in artificial intelligence (AI) processors, co-development of advanced commercial-off-the-shelf (COTS) programmable devices, and addressing select IP obsolescence risks; and 5) provide DoD's captive specialty needs suppliers and dedicated facilities with cost-effective upgrade capabilities and resources so they can deliver advanced technologies.

This project supports a broader national strategy to focus resources, policies, and incentives to enhance current and next generation defense capability by 1) maintaining access to U. S. domestic production of state-of-the-art (SOTA) technology; 2) enhancing state-of-the-practice (SOTP) foundries in the U.S. to produce more advanced technologies to better serve low-volume customers in the aerospace and defense community; 3) investing in research and development (R&D) for the next generation of microelectronics for new materials, devices, architectures, and designs in coordination with the Defense Advanced Research Projects Agency (DARPA) Electronics Resurgence Initiative (ERI); 4) promoting threat awareness, proactive protection, and supply chain security to ensure these investments continue to benefit the U.S.; 5) exploring incentives for market growth through dual-use technologies, piloting acquisition reforms, partnering with industry, and providing incentives for cooperative R&D and trade; and (6) establishing innovation hub pilots with industry.

MINSEC activities are categorized into the following focus areas: next generation disruptive R&D; capture and secure microelectronics R&D; new microelectronics development, demonstration, and capability insertion; COTS programmable integrated circuit (IC) co-development; microelectronics obsolescence and replacement; microelectronics-focused workforce development; radiation hardening by process (RHBP) and radiation hardening by design (RHBD); and radio frequency (RF) and optoelectronic (OE) microelectronics.

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

This project has received funding in FY 2020 to support MINSEC efforts in the following focus areas: capture and secure microelectronics R&D; new microelectronics development, demonstration, and capability insertion; RHBP and RHBD; and RF and OE microelectronics.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
Title: Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC)	0.000	147.749	459.170

Description: This project's activities will mature and evaluate microelectronics assurance technologies and techniques through efforts that may include the conduct of studies and Broad Agency Announcements (BAAs) and other efforts to coordinate research programs across USG R&D organizations, academia, and industry.

FY 2019 Plans:
This project will initiate and support R&D activities in each of the following technical focus areas:

• Capture and secure microelectronics R&D, including support and enhanced manufacturing at SOTP foundries.
• New microelectronics development, demonstration, and capability insertion including supporting public/private co-development of new COTS programmable devices that address USG needs during their development by industry when it is the most cost-effective to do so.
• RHBP and RHBD including supporting secure design of RHBD IP in all major domestic foundries and fabrication of SOTA test articles for evaluation and qualification.
• RF and optoelectronics including supporting secure design of IP and access to SOTP government and commercial facilities for RF and optical devices.

FY 2020 Plans:
This project will continue FY 2019 R&D activities in each of the following technical focus areas:

• Capture and secure microelectronics R&D, including support and enhanced manufacturing at SOTP foundries.
• New microelectronics development, demonstration, and capability insertion including supporting public/private co-development of new COTS programmable devices that address USG needs during their development by industry when it is the most cost-effective to do so.
• RHBP and RHBD including supporting secure design of RHBD IP in all major domestic foundries and fabrication of SOTA test articles for evaluation and qualification.
• RF and OE microelectronics including supporting secure design of IP and access to SOTP government and commercial facilities for RF and OE devices.
• Establish partnerships with industry for the following activities:

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2018	FY 2019	FY 2020
• Joint development of assured fifth-generation (5G) and internet of things (IoT) network, 5G modems, and end-user devices using assured design and fabrication processes; • Assured access to commercial foundry capabilities and products using assured design and fabrication processes and standards; • Joint development of assured processes and access to domestic assured memory with co-development of processing near-memory architectures and 3D integration for artificial intelligence and vision processing applications; • Assurance pilot with state-of-the-art foundry to adopt new assurance standards and methods to allow processing of U.S. government and critical commercial wafers in an assured commercial flow. This project will engage early on with potential stakeholders to identify potential transition issues and aid in transition through joint collaboration between research teams and stakeholders with a focus on evaluations of prototypes, test articles, and beta versions of tools, IP, techniques, methods, etc. and their use in operationally-realistic scenarios. ***FY 2019 to FY 2020 Increase/Decrease Statement:*** Prior the start of FY 2019, MINSEC activities were planned to be funded in Project Number 646. The funding for those MINSEC activities was subsequently reallocated to Project Number 647 during the first month of FY 2019. Level of effort is consistent between FY 2019 (including the congressional add) and FY 2020.			
Accomplishments/Planned Programs Subtotals	0.000	147.749	459.170

	FY 2018	FY 2019
Congressional Add: Next Generation Microelectronics	0.000	281.000
FY 2018 Accomplishments: N/A		
FY 2019 Plans: This project will use the Congressional Add funding in FY 2019 to support the following MINSEC activities: • Continue development of an advanced technology center for next-generation artificial intelligence systems. • Continue modernization enhancements for 90 nanometer (nm) to 65nm/45nm radiation-hardened semiconductor fabrication. • Provide robust access to advanced node foundry production and R&D processes and fully leverage the multiple domestic R&D facilities for DoD and national needs. • Deliver multiple secure design environments into industry, academia, and government to capture intellectual property (IP) and architectures and IP sharing and re-use.		

Exhibit R-2A, RDT&E Project Justification: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

	FY 2018	FY 2019
• Accelerate radiation-hardened processor design. • Continue development and expand deployment of a secure cloud environment and secure supply chain life cycle ecosystem.		
Congressional Adds Subtotals	0.000	281.000

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

E. Performance Metrics

Performance for this project is monitored in the following ways:

• Expanded access to leading SOTA technology and enhanced availability of essential SOTP design and fabrication capabilities.

• Successful transition demonstrations from commercial technology to modernized military applications, e.g., such as secure design environment suites and strategic radiation-hardened and RF-optical microelectronics.

• Successful development of new COTS devices including system-on-chip (SoC).

• Successful development of secure RHBP intellectual property in a major domestic foundry and enhanced manufacturing of integrated chips for evaluation and qualification.

• Successful development of RF and optoelectronic IP and test articles.

• Adoption of next-generation commercial technologies, as measured by:

- The number of DoD and other USG programs employing assured access to SOTP and SOTA technologies, design approaches, and best practices developed in cooperation with commercial partners.

- The volume and criticality of components employing these technologies, design approaches, or best practices.

Exhibit R-3, RDT&E Project Cost Analysis: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

Product Development ($ in Millions)

Cost Category Item	Contract Method & Type	Performing Activity & Location	Prior Years	FY 2018 Cost	FY 2018 Award Date	FY 2019 Cost	FY 2019 Award Date	FY 2020 Base Cost	FY 2020 Base Award Date	FY 2020 OCO Cost	FY 2020 OCO Award Date	FY 2020 Total Cost	Cost To Complete	Total Cost	Target Value of Contract
Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development	MIPR	DARPA, Air Force, Army, Navy, NSA : Various	-	-		428.749	Mar 2019	459.170	Mar 2020	-		459.170	Continuing	Continuing	-
		Subtotal	-	-		428.749		459.170		-		459.170	Continuing	Continuing	N/A

	Prior Years	FY 2018		FY 2019		FY 2020 Base		FY 2020 OCO		FY 2020 Total	Cost To Complete	Total Cost	Target Value of Contract
Project Cost Totals	-	-		428.749		459.170		-		459.170	Continuing	Continuing	N/A

Remarks

Exhibit R-4, RDT&E Schedule Profile: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

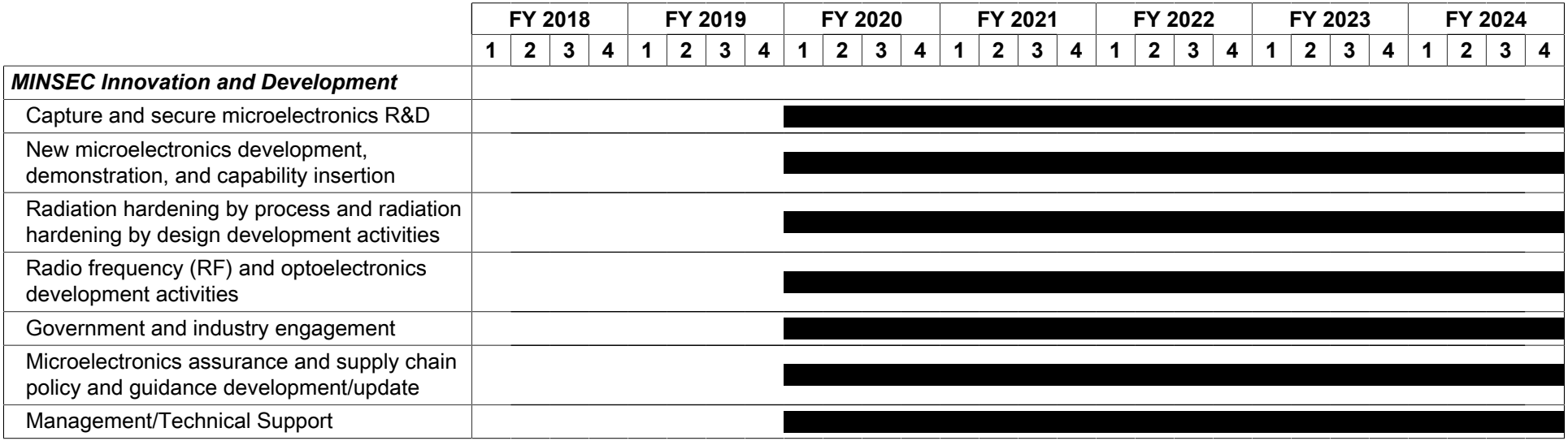

Exhibit R-4A, RDT&E Schedule Details: PB 2020 Office of the Secretary Of Defense		Date: February 2019
Appropriation/Budget Activity 0400 / 4	**R-1 Program Element (Number/Name)** PE 0604294D8Z / *Trusted and Assured Microelectronics*	**Project (Number/Name)** 647 / *Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC) Innovation and Development*

Schedule Details

	Start		End	
Events by Sub Project	**Quarter**	**Year**	**Quarter**	**Year**
MINSEC Innovation and Development				
Capture and secure microelectronics R&D	1	2020	4	2024
New microelectronics development, demonstration, and capability insertion	1	2020	4	2024
Radiation hardening by process and radiation hardening by design development activities	1	2020	4	2024
Radio frequency (RF) and optoelectronics development activities	1	2020	4	2024
Government and industry engagement	1	2020	4	2024
Microelectronics assurance and supply chain policy and guidance development/update	1	2020	4	2024
Management/Technical Support	1	2020	4	2024